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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/679,000	CHANG ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25 and 27-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25 and 27-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner..

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Amendments and Remarks filed on 2/14/2007 regarding application 10,679,000 filed on 10/02/2003.

2. Claims 1, 10-11, 21, 23 and 31 have been amended.

Claims 1-25 and 27-31 are pending for consideration.

3. ***Response to Amendments and Remarks***

Applicant's amendments and remarks have been fully and carefully considered, with the Examiner's response set forth below.

Response to Remarks on Double Patenting

Applicants contend that the provisioning double patenting rejection against Application 10/678,893 is not proper because the claims of 10/678,893 and 10/679,000 differ from one another. The Examiner disagrees with this assessment for the following reasons:

First, it is noted that Application 10/678,893 has recently been amended on 12/17/2006 with additional limitations.

Second, Examiner agrees that the scope of the claims of 10/678,893 and 10/679,000 are not the same. However, the fact that the scope of the claims of two applications are different does not necessarily exclude the possibility of double patenting between the two applications. As is well known, when two applications of the same invention have different scopes, the one of the narrower scope, i.e., with more limitations, would read on, hence teach, the one of the broader scope.

Third, for the cases of 10/678,893 and 10/679,000, both applications describe applying a first ECC algorithm to a first segment and a second ECC algorithm to a second segment of a non-volatile flash memory. Note that claims 4 and 6 of application 10/678,893 contains more limitations than that of application 10/679,000by associating segment/block 1 and segment/block 2 with an additional indicator. Thus although their claims appear to have different scope, the scope of 10/678,893 is narrower than, thus reads on, 10/679,000. Therefore, while Application 10/679,000 is subject to double patenting rejections against Application 10/678,893, Application 10/678,893 is not subject to double patenting rejections against Application 10/679,000. In other words, when two applications of the same invention have different scopes, the one of the narrower scope, i.e., with more limitations, would read on, hence teach, the one of the broader scope, but not the other way around.

Therefore, the provisional double patenting rejections are maintained in this Office Action.

Response to Amendments and Remarks on Amended Claims

In response, a new ground of claim analysis based on a newly identified reference (Katayama et al., US 6,651,212) in combination with a previously cited reference (Bassett et al., US 6,747,827) has been made. Refer to the corresponding sections of the claim analysis for details.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the

unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1, 3-4, 6-7, 10-11, 15, 21, 23, 27-28 and 31 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 4, 3, 6, 9 and 10 of copending Application No. **10/678,893** (most recently amended on 12/19/2006), as shown in the following table. Although not all of the conflicting claims are exactly identical, they are extremely similar and are not patentably distinct from each other, as explained in the "explanation" section below.

10/679,000	**10/678,893**
1. (currently amended) A method for storing data associated with a page within a non-volatile flash memory of a memory system, the page being the smallest unit of programming in the non-volatile	4 (currently amended) A method for storing data within a non-volatile memory comprised of a plurality of blocks in an array formed on a semiconductor substrate, each of the plurality of blocks having an indicator indicative of whether

flash memory, and having a data area and an overhead area, the method comprising: dividing at least a part of the page into at least a first segment and a second segment; encoding data associated with the first segment according to a first error correction code (ECC) algorithm; encoding data associated with the second segment according to a second error correction code (ECC) algorithm, wherein the second segment is encoded substantially separately from the first segment; programming the page with the encoded data associated with the first and second segments.	the block is a reclaimed block, the method comprising: identifying a first block of the plurality of blocks into which the data is to be stored; responsive to the indicator associated with the first block meeting a criterion, encoding the data using a first error detection algorithm; then writing the encoded data into the first block; identifying a second block of the plurality of blocks into which data is to be stored; responsive to the indicator associated with the second block not meeting the criterion, encoding the data using a second error detection algorithm, the second error detection algorithm having a higher error detection capability than the first error detection algorithm; and then writing the encoded data into the second block.
2. The method of claim 1 wherein the first segment includes the data area and the second segment includes the overhead area.	3. The method of claim 4 wherein the first error detection algorithm is a 1-bit error detection code (ECC) algorithm and the second algorithm is a 2-bit ECC algorithm.
3. The method of claim 1 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.	9. The method of claim 6 wherein the non-volatile memory is a flash memory.
4. The method of claim 1 wherein the first ECC calculations are associated with an ECC algorithm that is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.	10. The method of claim 9 wherein the flash memory is one of a NAND flash memory and an MLC NAND flash memory.
5. The method of claim 4 wherein the first ECC algorithm is a Hamming Code ECC algorithm.	6 (previously presented). A method for storing data within a non-volatile memory, comprised a plurality of blocks in an array formed on a semiconductor substrate, of a memory system, the method comprising: identifying one of the plurality of blocks into which the data is to be stored; obtaining an indicator associated with the identified block, the indicator having a value indicative of a number of times the first block has been erased; determining whether the indicator is less than a threshold value, responsive to the indicator being less than the threshold value, encoding the data using the first algorithm and then writing the data encoded using a first error detection algorithm into the identified block; responsive to the indicator not being less than the threshold value, encoding the data using a second algorithm and then writing the data encoded using a second error detection algorithm into the identified block, the second error detection algorithm having a higher error detection capability than the first error detection algorithm; repeating the identifying, obtaining, determining, encoding, and writing steps for another block in the array; wherein, as a result of the repeating step, a first block in the array stores data encoded according to the first algorithm, and a second block in the array stores data encoded according to the second algorithm.
6. The method of claim 1 wherein dividing the at	

least part of the page into the at least two segments of the data includes: dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment.	
7. The method of claim 6 further including: performing the ECC calculations on the third segment to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.	
8. The method of claim 6 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes the overhead area.	
9. The method of claim 6 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.	
10. The method of claim 1 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.	
11. A memory system comprising: a non-volatile memory, the non-volatile memory including a page, the page having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data; code devices for dividing at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment; code devices for performing error correction code (ECC) calculations on the first segment according to a first ECC algorithm to encode the first segment and on the second segment according to a second ECC algorithm to encode the second segment, wherein the second segment is encoded substantially separately from the first segment; and a memory area for storing the code devices.	
12. The memory system of claim 11 further including: a controller, the controller being arranged to process the code devices.	
13. The memory system of claim 11 wherein the first segment includes the data area and the second segment includes the overhead area.	
14. The memory system of claim 11 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.	
15. The memory system of claim 11 wherein the	

first ECC calculations are associated with an ECC algorithm that is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.	
16. The memory system of claim 15 wherein the first ECC algorithm is a Hamming Code ECC algorithm.	
17. The memory system of claim 11 wherein the code devices for dividing the at least part of the page into the at least two segments include: code devices for dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment.	
18. The memory system of claim 17 further including: code devices for performing the ECC calculations on the third segment according to one of the first and second ECC algorithm to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.	
19. The memory system of claim 17 wherein the first segment includes a first section of the data area, the third segment includes a second section of the data area, and the second segment includes the overhead area.	
20. The memory system of claim 17 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.	
21. The memory system of claim 11 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.	
22. The memory system of claim 11 wherein the code devices are one of software code devices and firmware code devices.	
23. A memory system comprising: a non-volatile memory, the non-volatile memory including a page, the page having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data; means that divide at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment; and means that perform error correction code (ECC) calculations on the first segment according to a first ECC algorithm to encode the first segment and on the second segment according to a second ECC algorithm to encode the second segment, wherein the second segment is encoded substantially	

separately from the first segment.	
24. The memory system of claim 23 wherein the first segment includes the data area and the second segment includes the overhead area.	
25. The memory system of claim 23 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.	
27. The memory system of claim 23 wherein the means that divide the at least part of the page into the at least two segments include: means that divide the page into three segments, the three segments including the first segment, the second segment, and a third segment.	
28. The memory system of claim 27 further including: means that perform the ECC calculations according to one of the first and second ECC algorithms on the third segment to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.	
29. The memory system of claim 27 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes the overhead area.	
30. The memory system of claim 27 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.	
31. The memory system of claim 23 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.	

10/679,000	10/678,893	EXPLANATION
1, 11 and 23	4, 6 and 9	Both describe applying a first ECC algorithm to a first segment and a second ECC algorithm to a second segment of a non-volatile flash memory; note that claims 4 and 6 of application 10/678,893 contains more limitations specifying how segment/block 1 and segment/block 2 are to be determined than application 10/679,000, thus 10/678,893 is narrower than, thus reads on, 10/679,000; also note that every non-volatile flash memory inherently has a smallest unit of programming, which may be referred to by various terms, such as page, sector, segment, block, or whatever.
3 and 15	3	Both recite a ECC algorithm that detects up to two incorrect bits and corrects up to one incorrect bit
6, 7, 27 and 28	4	Both recite the presence of a plurality of segments and the applications of ECC algorithm to each segment
10, 21 and 31	10	Both recite that the non-volatile memory is of NAND flash memory and MLC NAND flash memory

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3, 6-9, 11-14, 17-20, 22-25 and 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bassett et al. (US 6,747,827, hereinafter referred to as Bassett), and in view of Katayama et al. (US 6,651,212, hereinafter referred to as Katayama).

As to claim 1, Bassett discloses **a method for storing data associated with a page within a non-volatile flash memory of a memory system** [the corresponding "page" in Bassett's invention is a "track" of a disk memory (figure 3; column 2, lines 66-67 and column 3, lines 1-5; column 3, lines 21-25); Katayama teaches the aspect of a non-volatile flash memory disk, see below], **the page being the smallest unit of programming in the non-volatile flash memory** [every non-volatile flash memory inherently has a smallest unit of programming, which may be referred to by various terms, such as page, sector, segment, block, or whatever, since there is no standardized term in the art for "the smallest unit of programming"], **and having a data area and an overhead area** [The radial tracks may contain magnetic states that

contain information about the tracks, such as track identification data, location information, synchronization data, as well as user data (column3, lines 17-20); note that all data other than user data is overhead data]**, the method comprising**:

dividing at least a part of the page into at least a first segment and a second segment [a track is divided into a plurality of sectors (figure 3; column 2, lines 66-67 and column 3; column 4, lines 20-23)];

encoding data associated with the first segment according to a first error correction code (ECC) algorithm [For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract; column 6, lines 6-12; column 6, lines 39-47; column 4, lines 37-52)]; **and**

encoding data associated with the second segment according to a second error correction code (ECC) algorithm [For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract; column 6, lines 6-12; column 6, lines 39-47; column 4, lines 37-52)], **wherein the data associated with the second segment is encoded substantially separately from the data associated with the first segment** [abstract; column 3, lines 51-60; column 4, lines 37-52; column 6, lines 39-47].

Programming the page with the encoded data associated with the first and second segments [abstract; For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23)].

Regarding claim 1, the invention disclosed by Bassett et al. is applied toward a disk memory, which is non-volatile, but may or may not be a flash memory.

However, the method disclosed by Bassett et al. is equally applicable to a flash memory.

Further, Katayama et al. disclose in their invention "Recording/Reproduction device, Semiconductor memory, and Memory Card Using the Semiconductor Memory" a method of applying different ECC algorithms to different blocks of a flash memory disk [figure 1 shows the flash memory disk comprising flash memory element

(115~118), on-chip ECC (120~123) and ECC circuit (107); An ECC circuit implements a first error correction using a first BCH connection code and flash memory chips implement a second error connection using a second BCH error correction code which uses the same Galois filed (abstract)].

It is further noted that both Bassett et al. and Katayama et al. teach that the motivation of using different ECC algorithms to different blocks of memory instead of uniformly applying the same ECC algorithm to all blocks of memory is to save memory space [Bassett et al., y reducing the number of ECC bits that need be associated with at least some of the data to be written to the disk (12), the available space on the disk for user data can be increased (abstract); Katayama et al., It is known that a variable-length format scheme for a mass magnetic disk system uses a concatenated code to reduce redundant bytes of the error correction code so as to enhance the efficiency of error correction, as disclosed in Japanese Patent Unexamined Publications No. S59-165541, No. S62-73336 and No. H1-155721 (column 1, lines 38-43)].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the method disclosed by Bassett is equally applicable to a flash memory, as demonstrated by Katayama, and to incorporate the method disclosed by Bassett to a flash memory system as flash memory becomes more commonly used in the industries, as demonstrated by Katayama.

As to claim 2, Bassett teaches that **the first segment includes the data area** [the user data (The radial tracks may contain magnetic states that contain information about the tracks, such as track identification data, location information, synchronization

data, as well as user data (column3, lines 17-20); note that all data other than user data is overhead data)] **and the second segment includes the overhead area** [the overhead data includes track identification data, location information, synchronization data (The radial tracks may contain magnetic states that contain information about the tracks, such as track identification data, location information, synchronization data, as well as user data (column3, lines 17-20); note that all data other than user data is overhead data)].

As to claim 3, Bassett teaches that **the first segment includes a first section of the data area and the second segment includes a second section of the data area** [For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract].

As to claim 6, Bassett teaches that **dividing the at least part of the page into the at least two segments of the data includes**:

dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment [a track is divided into a plurality of sectors (figure 3; column 2, lines 66-67 and column 3; column 4, lines 20-23)].

As to claim 7, Bassett teaches that **performing the ECC calculations on the third segment according to one of the first and second ECC algorithms to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment** [For example, with reference again

to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract].

As to claim 8, Bassett teaches that **the first segment includes a first section of the data area, the third segment includes a second section of the data area** [For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract]**, and the second segment includes the overhead area** [the overhead data includes track identification data, location information, synchronization data (The radial tracks may contain magnetic states that contain information about the tracks, such as track identification data, location information, synchronization data, as well as user data (column3, lines 17-20); note that all data other than user data is overhead data)].

As to claim 9, Bassett teaches that **the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area** [a track is divided into a plurality of sectors (figure 3; column 2, lines 66-67 and column 3; column 4, lines 20-23); For example, with reference again to FIG. 3, a first error correcting code may be applied to data of a first type that is written to certain data sectors 80, and a second error correcting code may be applied to data of a second type that is written to other data sectors (column 7, lines 18-23); abstract].

As to claim 11, refer to "As to claim 1."

As to claim 12, Bassett teaches that **the memory system of claim 11 further including: a controller, the controller being arranged to process the code devices** [the microcontroller, figure 1, 32; figure 2; column 3, lines 39-42].

As to claim 13, refer to "As to claim 2."

As to claim 14, refer to "As to claim 3."

As to claim 17, refer to "As to claim 6."

As to claim 18, refer to "As to claim 7."

As to claim 19, refer to "As to claim 8."

As to claim 20, refer to "As to claim 9."

As to claim 22, Bassett teaches that **the code devices are one of software code devices and firmware code devices** [the ECC encoder (figure 2, 40) and the RLL encoder (figure 2, 42); column 3, lines 51-67].

As to claim 23, refer to "As to claim 1."

As to claim 24, refer to "As to claim 2."

As to claim 25, refer to "As to claim 3."

As to claim 27, refer to "As to claim 6."

As to claim 28, refer to "As to claim 7."

As to claim 29, refer to "As to claim 8."

As to claim 30, refer to "As to claim 9."

8. Claims 4-5, 15-16, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bassett et al. (US 6,747,827), in view of Katayama et al. (US

6,651,212, hereinafter referred to as Katayama), and further in view of Zhang et al. (US 6,662,333).

As to claim 4, neither Bassett nor Katayama explicitly mention that **the first ECC calculations are associated with an ECC algorithm is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment**.

However, Bassett does teach that the ECC library 510 typically contains a plurality of ECCs, including at least one weaker parity type code 512, at least one stronger BCH code 514, and at least one very strong Reed Solomon codes 516. To apply one of these ECCs to the redundancy 204 associated with the data structure 200, an appropriate divider similar to divider 206 may be selected to result in the required division between the payload and redundancy in the data structure 200 (column 7, lines 22-29).

Further, Applicants admit in the Background of the Invention Section of their disclosure that the above recited feature is well known in the art [some ECC algorithms that are used to encode and decode data for storage are known as 1-bit ECC algorithms and 2-bit ECC algorithms ... (paragraph 0009)].

Moreover, Zhang et al. disclose in their invention "Shared Error Correction for Memory Design" an ECC scheme in which single bit errors are corrected and double bit errors are detected [column 1, lines 24-33].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this

claim is well known in the art, as demonstrated by Applicants' admission as well as Zhang et al., hence lacking patentable significance.

As to claim 5, Bassett does not explicitly mention that **the ECC Algorithm is a Hamming Code ECC Algorithm**.

However, Bassett does teach that the ECC library 510 typically contains a plurality of ECCs, including at least one weaker parity type code 512, at least one stronger BCH code 514, and at least one very strong Reed Solomon codes 516. To apply one of these ECCs to the redundancy 204 associated with the data structure 200, an appropriate divider similar to divider 206 may be selected to result in the required division between the payload and redundancy in the data structure 200 (column 7, lines 22-29).

Further, Zhang et al. teach in their invention "Shared Error Correction for Memory Design" that Hamming Code based ECC algorithms are well known in the art [a well known error correction code is the Hamming code (column 1, lines 55-67)].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated Zhang et al., hence lacking patentable significance.

As to claim 15, refer to "As to claim 4."

As to claim 16, refer to "As to claim 5."

As to claim 26, refer to "As to claims 4-5."

9. Claims 10, 21 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bassett et al. (US 6,747,827), in view of Katayama et al. (US 6,651,212, hereinafter referred to as Katayama), and further in view of Kramer (US 6,182,239).

As to claims 10, 21 and 31, neither Bassett nor Katayama mention that **the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.**

However, the inventions of Bassett are directly applicable to any type of flash memories, including NAND flash memory and MLC NAND flash memory.

Further, Kramer teaches in the invention "Fault-Tolerant Codes for Multi-Level Memories" a fault-tolerant code semiconductor flash memory storage devices including an array of individual multi-level cell (MLC) storage devices [abstract; column 2, lines 1-15] as well as NAND flash memory [column 2, lines 36-57].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated Kramer, hence lacking patentable significance.

10. ***Related Prior Art On Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Shinohara, (US 5,742,934), "Flash Solid State Disk Card with Selective Use of An Address Conversion Table Depending on Logical and Physical Sector Numbers."

- Sukegawa et al., (US 5,603,001),"Semiconductor Disk system Having a Plurality of Flash Memories."
- Keays, (US Patent Application Publication 2003/0041210), "Erase Block Management."
- Carnevale et al., (US 6,353,910), "Method and Apparatus for Implementing Error Correction Coding (ECC) in a Dynamic Random Access Memory Utilizing Vertical ECC Storage."
- Yada et al., (US Patent Application Publication 2002/0032891), "Data processing System and Data Processing Method."
- Smith, (US 6,961,890), "Dynamic Variable-Length Error Correction Code."
- Payne et al., (US 2003/0099140), "Data Handling System."
- Benton et al., (US 5,164,944), "Method and Apparatus for Effecting Multiple Error Correction in a Computer Memory."
- Sinclair et al., (US Patent Application Publication 2003/0156473), "Memory Controller."
- Moro et al., (US 6,769,087), "Data Storage Device and Method for Controlling the Device."
- Purdham, (US 5,666,371), "Method and Apparatus for detecting Errors in a System that Employs Multi-Bit Wide Memory Elements."
- Kellogg et al., (US 5,896,404), "Programmable Burst Length DRAM."

Conclusion

11. Claims 1-25 and 27-31 are rejected as explained above.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

March 30, 2007

PIERRE BATAILLE
PRIMARY EXAMINER
3/30/07